

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

- 1 1. (Currently Amended) A memory device, comprising:
2 an array of [[a]] magnetic storage cells, each cell comprising a first magnetic
3 layer, a second magnetic layer, and a dielectric in between each said first
4 and second magnetic layers;
5 a first set of conductors to receive current for writing data to said magnetic
6 storage cells; and
7 a second set of conductors to provide a voltage across the second set of
8 conductors to cause current flow through at least one of the magnetic
9 storage cells for heating said at least one magnetic storage cell when
10 writing a bit of data to said at least one magnetic storage cell.

- 1 2. (Original) The memory device of claim 1, wherein the first set of conductors is
2 electrically isolated from the second set of conductors within the array of
3 magnetic storage cells.

- 1 3. (Currently Amended) The memory device of claim 1, wherein heating said at
2 least one magnetic storage cell reduces the magnetic coercivity of at least
3 one of the first and second magnetic layers ~~comprising~~ of the magnetic
4 storage cell.

- 1 4. (Original) The memory device of claim 1, wherein the array of magnetic storage
2 cells comprise spin tunneling storage cells.

- 1 5. (Original) The memory device of claim 1, wherein the array of magnetic storage
2 cells comprise giant magnetoresistive storage cells.

- 1 6. (Original) The memory device of claim 1, wherein said array of magnetic storage
2 cells comprise anisotropic magnetoresistive material.

1 7. (Original) The memory device of claim 1, wherein said array of magnetic storage
2 cells comprise any magnetoresistive storage material.

1 8. (Original) The memory device of claim 1 wherein said magnetic storage cells
2 serve as electrical heating elements.

1 9. (Cancelled)

1 10. (Original) The memory device of claim 1, wherein said second conductor set
2 includes a heater element placed in series with at least one of the
3 conductors of the second conductor set.

1 11. (Original) The memory device of claim 10, wherein said heater element is a
2 resistive device.

1 12. (Currently Amended) ~~The memory device of claim 1,~~ A memory device,
2 comprising:
3 an array of magnetic storage cells, each cell comprising a first magnetic layer, a
4 second magnetic layer, and a dielectric in between each said first and
5 second magnetic layers;
6 a first set of conductors to receive current for writing data to said magnetic
7 storage cells;
8 a second set of conductors for heating at least one magnetic storage cell when
9 writing a bit of data to said at least one magnetic storage cell; and
10 ~~wherein said magnetic memory device includes~~ a heater element placed in series
11 with the at least one ~~of the said~~ magnetic storage cells cell.

1 13. – 18. (Cancelled)

1 19. (Currently Amended) An electronic device comprising:
2 a processor;
3 an input device coupled to said processor;
4 an output device coupled to said processor;
5 and a memory device coupled to said processor, wherein said memory device
6 comprises[[;]]:
7 an array of a magnetic storage cells, each ~~region~~ magnetic storage cell
8 comprising a first magnetic layer, a second magnetic layer, and a
9 dielectric in between each said first and second magnetic layers;
10 a first set of conductors to receive current for writing data to said magnetic
11 storage cells; and
12 a second set of conductors for applying a voltage across said at least one
13 magnetic storage cell for heating said at least one magnetic storage
14 cell prior to writing a bit of data to said at least one magnetic
15 storage cell.

1 20. (Original) The electronic device of claim 19, wherein the array of magnetic
2 storage cells comprise random access memory.

1 21. (Original) The electronic device of claim 19, wherein said first magnetic layer
2 has a fixed orientation of magnetization and the second layer has a non-
3 fixed orientation.

1 22. (Original) The electronic device of claim 19, wherein at least one of said second
2 set of conductors includes a resistive heating element for heating each
3 magnetic storage cell when current flows through said heating element.

1 23. (Currently Amended) A magnetic storage cell comprising;
2 a first magnetic layer, a second magnetic layer, and a dielectric in between said
3 first and second magnetic layers;
4 a first set of conductors positioned above and below said first and second
5 magnetic layers for writing to said magnetic storage cell; and
6 a second set of conductors positioned above and below said first and second
7 magnetic layers for applying a voltage across [[a]] said magnetic storage
8 cell for heating said ~~selected~~ magnetic storage cell prior to writing a bit of
9 data to said magnetic storage cell and for reading the data bit that is stored
10 on said magnetic storage cell.

1 24. (Original) The magnetic storage cell of claim 23, wherein said magnetic storage
2 cell is a spin tunneling storage cell.

1 25. (New) The memory device of claim 1, wherein the first set of conductors is
2 separate from the second set of conductors.

1 26. (New) The memory device of claim 1, wherein the first and second magnetic
2 layers and the dielectric of the at least one magnetic storage cell and the
3 first and second set of conductors are arranged in a stack,
4 wherein the second set of conductors is located between the first set of conductors
5 in the stack.

1 27. (New) The memory device of claim 26, the second set of conductors to further
2 provide a read voltage across the second set of conductors to read the at
3 least one magnetic storage cell during a read operation.

1 28. (New) The memory device of claim 1, the second set of conductors to further
2 provide a read voltage across the second set of conductors to read the at
3 least one magnetic storage cell during a read operation.

1 29. (New) The electronic device of claim 19, wherein the first set of conductors is
2 separate from the second set of conductors.

1 30. (New) The electronic device of claim 19, wherein the first and second magnetic
2 layers and the dielectric of the at least one magnetic storage cell and the
3 first and second set of conductors are arranged in a stack,
4 wherein the second set of conductors is located between the first set of conductors
5 in the stack.

1 31. (New) The electronic device of claim 30, the second set of conductors to further
2 provide a read voltage across the second set of conductors to read the at
3 least one magnetic storage cell during a read operation.

1 32. (New) The electronic device of claim 19, the second set of conductors to further
2 provide a read voltage across the second set of conductors to read the at
3 least one magnetic storage cell during a read operation.

1 33. (New) The magnetic storage cell of claim 23, wherein the first and second
2 magnetic layers, dielectric, first set of conductors, and second set of
3 conductors are arranged in a stack, and
4 wherein the second set of conductors is located between the first set of conductors
5 in the stack.